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August 29, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Technology Center 2100

SUBJECT: Applicants: Stein et al.
Serial No: 10/090,941
Filed: March 5, 2002
For: SINGLE INSTRUCTION MULTIPLE DATA ARRAY CELL

Group No: 2183
Docket No: AD-303J

Dear Sir:

Pursuant to 37 CFR §1.56, enclosed are an Information Disclosure Citation in an Application, Form PTO-A820, and copies of thirty-seven (37) references.

This Information Disclosure Citation is timely filed and should be considered as it is filed before the mailing date of the first Office Action on the merits of the subject application pursuant to 37 CFR §1.97(b)(3).

If at any time it appears that a TELEPHONE CONFERENCE with counsel would help advance prosecution, please telephone the undersigned, or his associates, collect in Waltham, Massachusetts, at. (781) 890-5678.

If any payment during prosecution is found to be incorrect, please charge any deficiency or credit any overpayment to by Deposit Account No. 09-0002. A copy of this letter is enclosed for use by the Finance Branch in the event that it is necessary to make any charge or credit to my deposit account.

Kindly acknowledge receipt of the foregoing by returning the enclosed self-addressed postcard.

Sincerely,

R. Stephen Rosenholm
Reg. No. 45,283

RSR:wj
Enclosures

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 29, 2003.

Wynne D. Janis

INFORMATION DISCLOSURE CITATION

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Art Unit

2183

U.S. PATENT DOCUMENTS

| *EXAMINER INITIALS | REF | DOCUMENT NUMBER | PUBLICATION DATE | NAME OF PATENTEE OR APPLICANT | FILING DATE IF APPROPRIATE |
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| 13 | Viktor Fischer, <i>Realization of the Round 2 AES Candidates Using Altera FPGA</i> , (January 26, 2001) < http://csrc.nist.gov/CryptoToolkit/aes/roun2/conf3/papers/24-vfischer.pdf > (Micronic - Kosice, Slovakia). |
| 14 | Máire McLoone and J.V. McCanny, <i>High Performance Single-Chip FPGA Rijndael Algorithm Implementations</i> , CHES 2001 PROC, LNCS 2162, 65-76 (Ç.K. Koç et al. eds. 16 May 2001). |

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| 37 | PACT Informationstechnologie GmbH, <i>The XPP White Paper Release 2.1</i> (March 27, 2002) < http://www.pactcorp.com/xneu/download/xpp_white_paper.pdf > (PACT XPP - Santa Clara, CA). |

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